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# EXHIBIT E

(12) **INTER PARTES REEXAMINATION CERTIFICATE** (1643rd)

**United States Patent**

**Bhakta et al.**

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(54) **MEMORY MODULE DECODER**

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**H05K 1/18** (2006.01)

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(52) **U.S. Cl.**

CPC ..... **GIIC 8/12** (2013.01); **G06F 12/0207** (2013.01); **G06F 12/0215** (2013.01); **GIIC 5/04** (2013.01); **GIIC 5/066** (2013.01); **GIIC 7/1048** (2013.01); **H05K 1/181** (2013.01); **GIIC 2207/105** (2013.01); **H05K 2201/10159** (2013.01); **H05K 2203/1572** (2013.01); **Y02P 70/50** (2015.11)

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(58) **Field of Classification Search**

None

See application file for complete search history.

(56) **References Cited**

To view the complete listing of prior art documents cited during the proceedings for Reexamination Control Numbers 95/001,339, 95/000,578 and 95/000,579, please refer to the USPTO's public Patent Application Information Retrieval (PAIR) system under the Display References tab.

*Primary Examiner* — B. James Peikari

(57) **ABSTRACT**

A memory module connectable to a computer system includes a printed circuit board, a plurality of memory devices coupled to the printed circuit board, and a logic element coupled to the printed circuit board. The plurality of memory devices has a first number of memory devices. The logic element receives a set of input control signals from the computer system. The set of input control signals corresponds to a second number of memory devices smaller than the first number of memory devices. The logic element generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices.

Certificate of Correction issued Aug. 10, 2010

**Related U.S. Application Data**

(63) Continuation of application No. 11/173,175, filed on Jul. 1, 2005, now Pat. No. 7,289,386, and a continuation-in-part of application No. 11/075,395, filed on Mar. 7, 2005, now Pat. No. 7,286,436.

(60) Provisional application No. 60/588,244, filed on Jul. 15, 2004, provisional application No. 60/550,668, filed on Mar. 5, 2004, provisional application No. 60/575,595, filed on May 28, 2004.

(51) **Int. Cl.**

**GIIC 15/02** (2006.01)

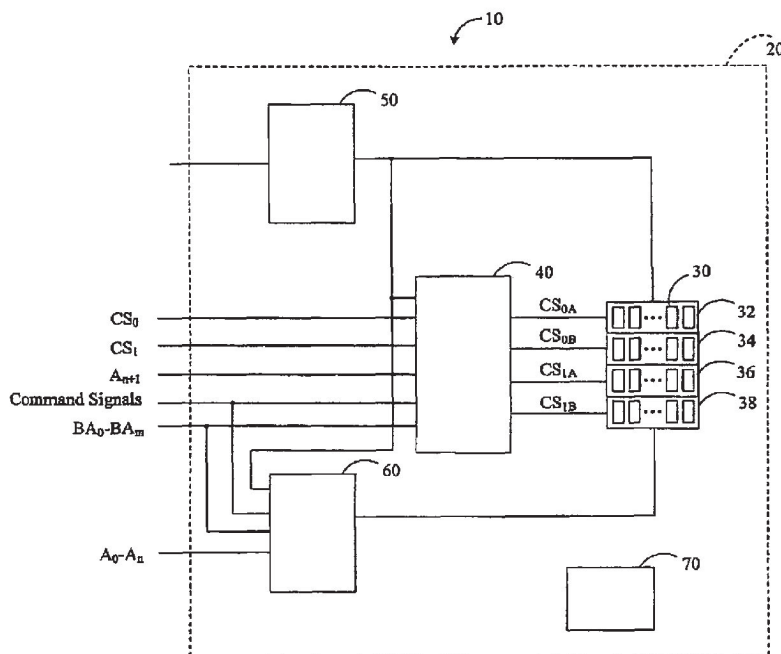
**GIIC 7/10** (2006.01)

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**GIIC 5/04** (2006.01)



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**INTER PARTES**

**REEXAMINATION CERTIFICATE**

THE PATENT IS HEREBY AMENDED AS  
INDICATED BELOW.

**Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.**

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

Claims **2, 5, 7, 9, 21, 23, 25, 26, 30, 33, 42, 44** and **51** are cancelled.

Claims **1, 15, 16, 28, 39** and **43** are determined to be patentable as amended.

Claims **3, 4, 6, 8, 10-14, 17-20, 22, 24, 27, 29, 31, 32, 34-38, 40, 41** and **45-50**, dependent on an amended claim, are determined to be patentable.

New claims **52-91** are added and determined to be patentable.

**1.** A memory module connectable to a computer system, the memory module comprising:

- a printed circuit board;
- a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;
- a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and
- a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

*wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register;*

*wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and*

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*the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element, and*

*wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response to at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal.*

**15.** A memory module connectable to a computer system, the memory module comprising:

- a printed circuit board;
- a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;
- a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and
- a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

*wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register;*

*wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the at least one DDR memory device of the selected one or two ranks of the first number of ranks, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are*



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separate from the at least one row address signal received by the logic element, and wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals and (iii) the at least one chip-select signal of the set of input signals and (iv) the PLL clock signal.

16. [The memory module of claim 15] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;  
a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;  
a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and  
a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,  
wherein the command signal is transmitted to only one DDR memory device at a time.

28. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;  
a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;  
a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first

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number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register,

wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR DRAM memory devices, the logic element, and the register,

wherein, the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the at least one DDR DRAM device of the selected at least one rank, wherein the row/column address signal received by the logic element comprises a row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the row address signal received by the logic element, and

wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the row address signal, (ii) the bank address signals, and (iii) the chip-select signal of the set of input control signals and (iv) the PLL clock signal.

39. A memory module connectable to a computer system, the memory module comprising:

a printed circuit board having a first side and a second side;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or more ranks which are selectable by a first number of chip-select signals; and

at least one integrated circuit element mounted to the printed circuit board, the at least one integrated circuit element comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the at least one integrated circuit element receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives at least one row address signal, the bank address signals, at least one chip-select signal, and at least one command signal of the plurality of input signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals, the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one